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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,622	10/27/2000	Jyh-Ming Jong	P4928/06145.003001	4922

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/698,622	Applicant(s) JONG ET AL.	
	Examiner Emmanuel Bayard	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed 10/26/04 in which claims 1-7 and 9-13 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-6, 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hastings et al U.S. Patent No 6,275,074 B1.

As per claims 1 and 9, Hastings discloses an apparatus for detecting a noise error of a signal comprising: an high comparator (see figs.3-55, element 84 and col.5, lines 10-67 and col.8, lines 16-55) that references a high voltage limit with the signal and generates an output; a low comparator (see figs.3-5, element 86 and col.5, lines 10-67 and col.8, lines 30-50) that references a low voltage limit with the signal and generates an output; and a circuit (see figs.3-5 elements 88 and 92 are combined to form the claimed "circuit" and col.5, lines 15-25) that processes the high comparator output and the low comparator output, wherein at least one of the high comparator output and at least one of low comparator

output clocks (see figs.3-5 element C) the circuit and wherein the circuit generates an emitting light is considered as the claimed (alarm) if a noise error is detected (see col.5, lines 18-65 and col.6, lines 1-67) .

As per claim 2, the apparatus of Hastings does include a high-to-low sub-circuit that detects a noise error during a (1)(rising) signal transition and a low-to-high sub-circuit that detects a noise error during a (0)(falling) signal transition (see figs.3-5 element 90 and col.5, lines 15-67).

As per claim 4, the apparatus of Hastings does include a differential amplifier (see fig.5 element 104 or 150 or 162).

As per claim 5, the apparatus of Hastings inherently includes a sense amplifier.

As per claims 6 and 10, the apparatus of Hastings inherently includes high voltage limit and the low voltage limit is 30 mV.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3, 7, 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hastings U.S. Patent No 6,275,074 in view of Nemetz et al U.S. patent No 5,923,191.

As per claim 3, Hastings teaches all the features of the claimed invention including a belay buffer (see col.3, lines 54-60 and col.7, lines 15-25); a flip-flop circuit (see col.5, line 17) and an XOR logic gate (see col.5, line 63).

However Hastings does not teach a plurality of flip-flop circuits Nemezt et al teaches a plurality of flip-flop circuits (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65) and logic gate (see figs.7A-7B elements 80, 80a and col.11, line 58-67 and col.12, lines 1-67).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Hastings as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

As per claims 7 and 13, Hastings teaches discloses an apparatus for detecting a noise error of a signal comprising: an high comparator (see figs.3-55, element 84 and col.5, lines 10-67 and col.8, lines 16-55) that references a high voltage limit with the signal and generates an output; a low comparator (see figs.3-5, element 86 and col.5, lines 10-67 and col.8, lines 30-50) that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 30 mV; and a high and low circuit and a low-to-high sub-circuit that detects a noise error during a falling signal transition (see figs.3-5 element 90 and col.5, lines 15-67) that detects a noise error during a rising and falling signals transition wherein the sub-circuit generates an emitting light is considered as the claimed (alarm) if a noise error is detected; a delay buffer (see col.3, lines 54-60 and col.7, lines 15-

25); a flip-flop circuit (see col.5, line 17) and an XOR logic gate (see col.5, line 63) wherein at least one of the high to-low sub-circuit and the low-to-high sub-circuit generates an alarm if a noise error is detected (see col.5, lines 20-67 and col.6, lines 1-67).

However Hastings does not teach either sub-circuit comprises a plurality of flip-flop circuits.

Nemezt teaches sub-circuit comprises a plurality of flip-flop circuits (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Hastings as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

As per claims 11 and 12, Hastings teaches all the features of the claimed invention except a plurality of flip-flops.

Nemezt et al teaches a sub-circuit plurality of flip-flop circuits (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Hastings as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stuebing et al U.S. patent No 5,097,147 teaches a limited amplitude signal trigger (***).

Parle et al U.S. Patent No 5,498,985 teaches a dual comparator trigger circuit.

Dent U.S. patent No 6,108,808 teaches an apparatus and method for decoding.

Hashimoto et al U.S. patent No 5,295,132 teaches a multiplex transmission apparatus.

Kato et al U.S. patent No 6,188,829 B1 teaches a data reproduction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

2/24/05

EMMANUEL BAYARD
PRIMARY EXAMINER